SPNYPM-52832-P02 Bluetooth 4.2 Low Energy Module

Datasheet

SPINTLY

NAME: Bluetooth 4.2 Low energy Module

MODEL NO: SPNYPM01

VERSION: P02

CONTENTS

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1. Revision History

Revision	Description	Author	Approval	Date
P01	Initial Release	Sneha	Brosnan	14-10-2019
P02	Updated section 14.1 with layout notes	Sneha	Brosnan	23-12-2019

2. Product Description

SPNYPM-52832-P02 is powerful, highly flexible, ultra-low power Bluetooth Low Energy 4.2 (BLE 4.2) modules using Nordic nRF52832 SoCs. It was designed for high data rate, short-range wireless communication in the 2.4GHz ISM band. With an ARM CortexTM M4F MCU, available 512KB flash, 64KB RAM, embedded 2.4GHz multi-protocol transceiver, power amplifier, and an integrated 2.4GHz Mini antenna or an UFL connector for external antenna.
The SPNYPM-52832-P02 is a 16.5 mm × 23 mm module with antenna. It allows developers to take full advantage of the nRF52832 by making all its I/O available via 36 SMD 1.1mm pitch pads.
Four GPIOs are used to control power amplifier. Other GPIOs of nRF52832 can be accessed from main board.

3. Product Classification

Model No	Antenna	Module	
		SoC	Flash/RAM
SPNYPM01	Chip Antenna	nRF52832-QFAA	512KB/64KB

4. Key Features

- 21 dBm maximum output power
- Range of communication up to 250m
- 32 bits ARM® Cortextm-M4 @ 16MHz
- 2.4GHz multi-protocol transceiver
- 64KB SRAM
- 512KB Flash
- 32 configurable I/O pins, 19 General Purpose I/O pins
- One 32 and two 16 bit timers with counter mode
- 20 channel CPU independent Programmable Peripheral Interconnect (PPI)
- Encryption -128 bit AES ECB/CCM/AAR co-processor
- RNG, RTC
- Temperature sensor
- Digital interfaces SPI Master/Slave, 2-wire Master (I2C compatible), UART
- (CTS/RTS), IIS, PDM
- Quadrature decoder
- 12bit 200KSPS ADC - 8 configurable channels
- -96dBm sensitivity
- Option available of UFL for external antenna

5. Applications

- Beacons
- Bluetooth Gateway
- RTLS (Real-Time Location System)
- Smart Indoor/Outdoor Lighting
- Smart Access Control system

6. Application Block Diagram

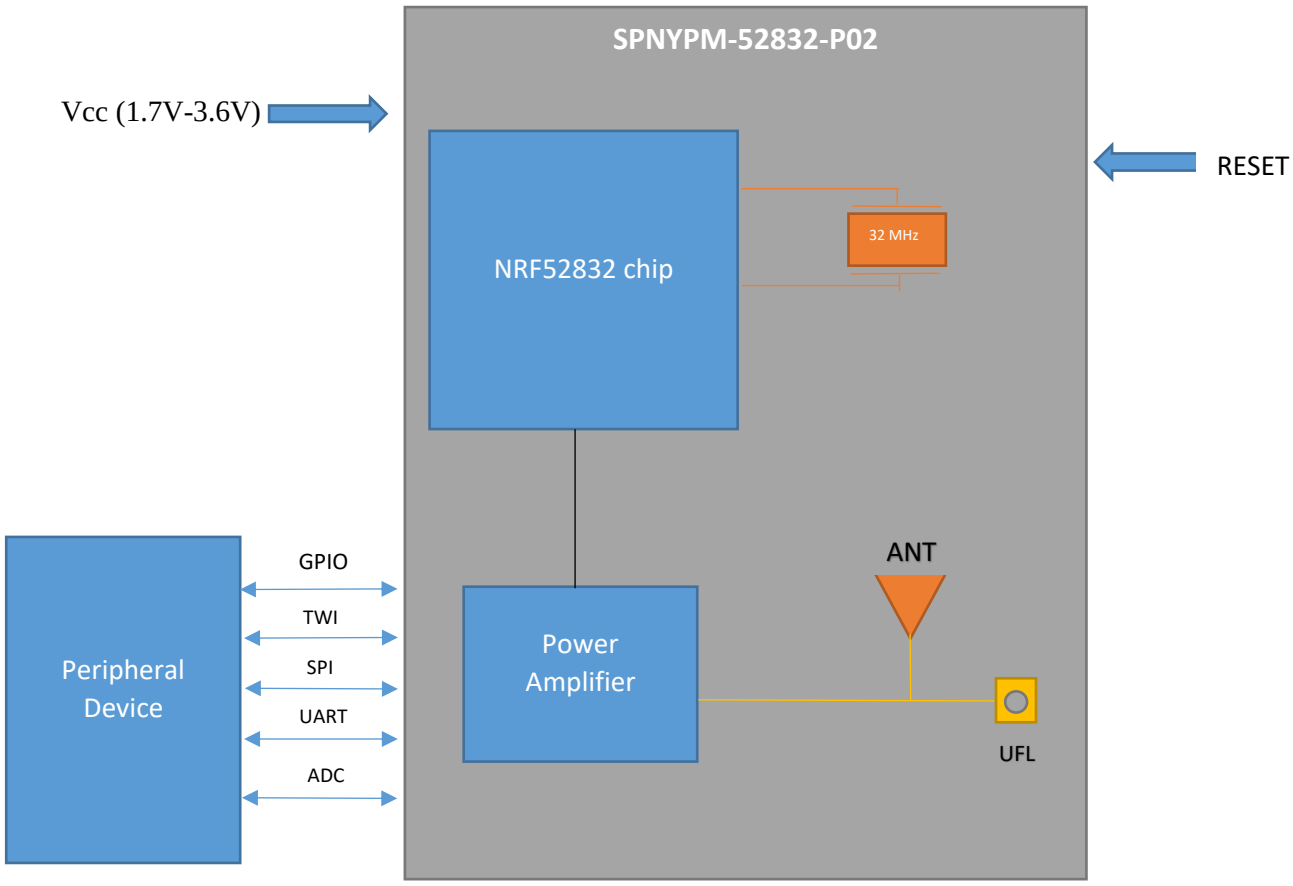


Figure 1: SPNYPM-52832-P02 Block diagram

7. Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time
without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

	Min.	Max.	Unit
Supply voltages			
VCC	1.7	3.6	V
VSS		0	
I/O pin voltage			
VI/O, VDD ≤3.6 V	-0.3	VDD + 0.3 V	V
VI/O, VDD >3.6 V	-0.3	3.9V	V
NFC antenna pin current			
INFC1/2		80	mA
Environmental 36-SMD package			
Storage temperature	-40	+125	°C

8. Recommended Operating Conditions

The operating conditions are the physical parameters that the chip can operate within.

Symbol	Parameter	Min.	Nom.	Max.	Units
VCC	Supply voltage, independent of DCDC enable	1.7	3.3	3.6	V
TA	Operating temperature	-40	25	85	°C
TR_VDD	Supply rise time (0 V to 1.7 V)			60	ms

9 Electrical specification

9.1 Current consumption, sleep

Symbol	Description	Min.	Typ.	Max.	Units
IOFF	System OFF current, no RAM retention		0.3		µA
ION	System ON base current, no RAM retention		1.2		µA
IRAM	Additional RAM retention current per 4 KB RAM section		20		nA

9.2 Device start-up times

Symbol	Description	Min.	Typ.	Max.	Units
tPOR	Time in Power on Reset after VDD reaches 1.7 V for all supply voltages and temperatures. Dependent on supply rise time. 10				
tPOR,10us	VDD rise time 10us		1		ms
tPOR,10ms	VDD rise time 10ms		9		ms
tPINR	If a GPIO pin is configured as reset, the maximum time taken to pull up the pin and release reset after power on reset. Dependent on the pin capacitive load (C)11: t=5RC, R = 13kOhm		23		ms
tPINR,500nF	C = 500nF			32.5	ms
tPINR,10uF	C = 10uF			650	ms
tR2ON	Time from reset to ON (CPU execute)				
tR2ON,NOTCONF	If reset pin not configured	tPOR			ms
tR2ON,CONF	If reset pin configured	tPOR + tPINR			ms
tOFF2ON	Time from OFF to CPU execute		16.5		µs
tIDLE2CPU	Time from IDLE to CPU execute		3.0		µs
tEVTSET,CL1	Time from HW event to PPI event in Constant Latency System ON mode		0.0625		µs
tEVTSET,CL0	Time from HW event to PPI event in Low Power System ON mode		0.0625		µs

10. Interfaces

10.1 Power Supply

Regulated power for the SPNYPM-52832-P02 is required. The input voltage Vcc range should be 1.7V to 3.6V. Suitable decoupling must be provided by external decoupling circuitry (1uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

10.2 System Function Interfaces

10.2.1 GPIOs

Each GPIO can be accessed
individually with the following user configurable features:

◆Input/output direction
◆Output drive strength
◆Internal pull-up and pull-down resistors
◆Wake-up from high or low-level triggers on all pins
◆Trigger interrupt on all pins
◆All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
◆All pins can be individually configured to carry serial interface or quadrature demodulator signals
◆All pins can be configured as PWM signal
◆There are 6 ADC/LPCOMP input in the 19 I/O s

10.2.2 Two-wire Interface (I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps ,250kbps and 400 kbps. The module has 2 TWI ports and they properties like following table.

Instance	Master/Slave
TWI 0	Master
TWI 1	Master

Table 1: TWI Pins share scheme

Note： I2C: Inter－Integrated Circuit

10.2.3 Flash Program I/O s

The module has two programmer pins, respectively SWDCLK pin and SWDIO pin. The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for nonintrusive debugging of program code. Breakpoints and single stepping are part of this support.

10.2.4 Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip selects signal for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The GPIOs are used for each SPI interface line can be chosen from any GPIOs on the device and independently. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.
The SPI peripheral support SPI mode 0,1,2, and 3. The module have 3 SPI ports and theirs they properties are as below:

Instance	**Master/Slave**
SPI 0	Master
SPI 1	Master
SPIS 1	Slave

Table 2: SPI Properties

10.2.5 UARTs

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS), support in hardware up to 1 Mbps baud. Parity checking is supported.
Support the following baud rate in bps unit:
1200/2400/4800/9600/14400/19200/28800/38400/57600/76800/115200.
Note: The GPIOs are used for each SPI/TWI/UART interface line can be chosen from any GPIOs on the device and configed independently.

10.2.6 Analog to Digital Converter (ADC)

The 12-bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8,10, and 12 bit).

Note: The ADC module uses the same analog inputs as the LPCOMP module. Only one of the modules can be enabled at the same time.

SPNYPM-52832-P02 Pin Number	Pin Number	Description
5	P0.28	General Purpose I/O, SAADC/COMP/LPCOMP input
6	P0.29	General Purpose I/O, SAADC/COMP/LPCOMP input
7	P0.30	General Purpose I/O, SAADC/COMP/LPCOMP input
8	P0.31	General Purpose I/O, SAADC/COMP/LPCOMP input
13	PO.02	General Purpose I/O, SAADC/COMP/LPCOMP input
14	PO.03	General Purpose I/O, SAADC/COMP/LPCOMP input
15	PO.04	General Purpose I/O, SAADC/COMP/LPCOMP input
16	PO.05	General Purpose I/O, SAADC/COMP/LPCOMP input

Table 3: ADC Pins

10.2.7 Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

10.2.8 Reset

The reset pin of the SPNYPM-52832-P02 module is in the internal pull-high state, when the reset pin of the module is input to a low level, the module will be automatically reset. After the reset pin is used, the parameters of the current setting will not be reserved.

11. Module Pinout and Pin Description

11.1 Module Pinout

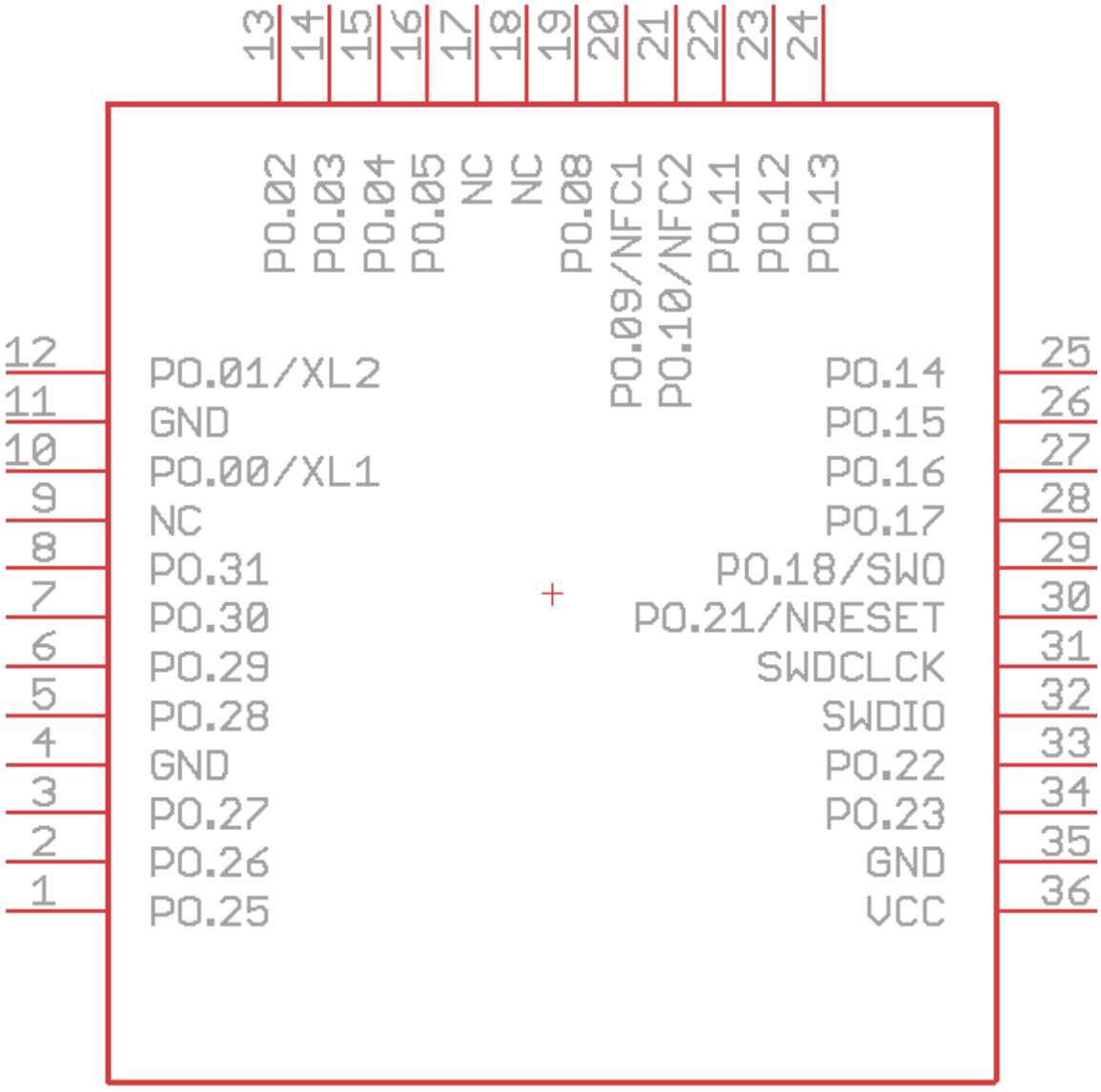


Figure 2: SPNYPM-52832-P02 Module Pinout

11.2 Pin Description

BLE PA Module Pin Number	BLE PA Module Pin Name	nRF52832 QFN Pin Number	nRF52832 QFN Pin Name	Pin Function	Comments
1	PO.25	37	PO.25	General Purpose I/O	GPIO available
2	PO.26	38	PO.26	General Purpose I/O	GPIO available
3	PO.27	39	PO.27	General Purpose I/O	GPIO available
4	GND	Multiple	GND	Ground	
5	PO.28	40	P0.28	General Purpose I/O, SAADC/COMP/LPCOMP input	GPIO available
6	PO.29	41	P0.29	General Purpose I/O, SAADC/COMP/LPCOMP input	GPIO available
7	PO.30	42	P0.30	General Purpose I/O, SAADC/COMP/LPCOMP input	GPIO available
8	PO.31	43	P0.31	General Purpose I/O, SAADC/COMP/LPCOMP input	GPIO available
9	N.C.	29	P0.24	General Purpose I/O	N.C.
10	PO.00	2	PO.00/XL1	General Purpose I/O, Connection for 32.768 kHz crystal (LFXO)	GPIO available/32.768k crystal
11	GND	Multiple	GND	Ground	
12	PO.01	3	PO.01/XL2	General Purpose I/O, Connection for 32.768 kHz crystal (LFXO)	GPIO available/32.768k crystal
13	PO.02	4	PO.02	General Purpose I/O, SAADC/COMP/LPCOMP input	GPIO available
14	PO.03	5	PO.03	General Purpose I/O, SAADC/COMP/LPCOMP input	GPIO available
15	PO.04	6	PO.04	General Purpose I/O, SAADC/COMP/LPCOMP input	GPIO available
16	PO.05	7	PO.05	General Purpose I/O, SAADC/COMP/LPCOMP input	GPIO available
17	PO.06	8	PO.06	General Purpose I/O	connected to PA
18	PO.07	9	PO.07	General Purpose I/O	connected to PA
19	PO.08	10	P0.08	General Purpose I/O	GPIO available
20	PO.09	11	NFC1/P0.09	General purpose I/O, NFC antenna connection	

21	PO.10	12	NFC2/P0.10	General purpose I/O, NFC antenna connection	
22	PO.11	14	P0.11	General Purpose I/O	GPIO available
23	PO.12	15	P0.12	General Purpose I/O	GPIO available
24	PO.13	16	P0.13	General Purpose I/O	GPIO available
25	PO.14	17	P0.14	General Purpose I/O, Trace port output	GPIO available
26	PO.15	18	P0.15	General Purpose I/O, Trace port output	GPIO available
27	PO.16	19	P0.16	General Purpose I/O, Trace port output	GPIO available
28	PO.17	20	P0.17	General Purpose I/O	GPIO available
29	PO.18/SWO	21	P0.18/SWO	General purpose I/O, Single wire output, Trace port output	used for programming
30	NRESET/PO.21	24	P0.21/NRESET	General purpose I/O, Configurable as pin reset	used for programming
31	SWDCLCK	25	SWDCLK	Serial wire debug clock input for debug and programming	used for programming
32	SWDIO	26	SWDIO	Serial wire debug I/O for debug and programming	used for programming
33	PO.22	27	P0.22	General Purpose I/O	GPIO available
34	PO.23	28	P0.23	General Purpose I/O	GPIO available
35	GND	Multiple	GND	Ground	Ground
36	VCC	Multiple	VCC	Power Supply	Power Supply
		1	DEC_1	0.9 V regulator digital supply decoupling	
		13	VDD	Power supply	Power supply
		22	P0.19	General purpose I/O	connected to PA
		23	P0.20	General purpose I/O	connected to PA
		30	ANT RF	Single-ended radio antenna connection	
		31	VSS	Power Ground (Radio supply)	
		32	DEC_2	Power 1.3 V regulator supply decoupling (Radio supply)	
		33	DEC_3	Power supply decoupling	
		34	XC1	Connection for 32 MHz crystal	32 MHz crystal
		35	XC2	Connection for 32 MHz crystal	32 MHz crystal
		36	VDD	Power supply	
		44	NC	NC	N.C.
		45	VSS	Ground	Ground

		46	**DEC_4**	**1.3 V regulator supply decoupling**	
		47	**DCC**	**DC/DC regulator output**	
		48	**VDD**	**Power supply**	**Power supply**

12. PCB Design Guide

Reserve empty area for PCB antenna when you are going to design a device's board.

The empty range minimum size: 16.5 mm X 7.00 mm. Check the figure below for reference.

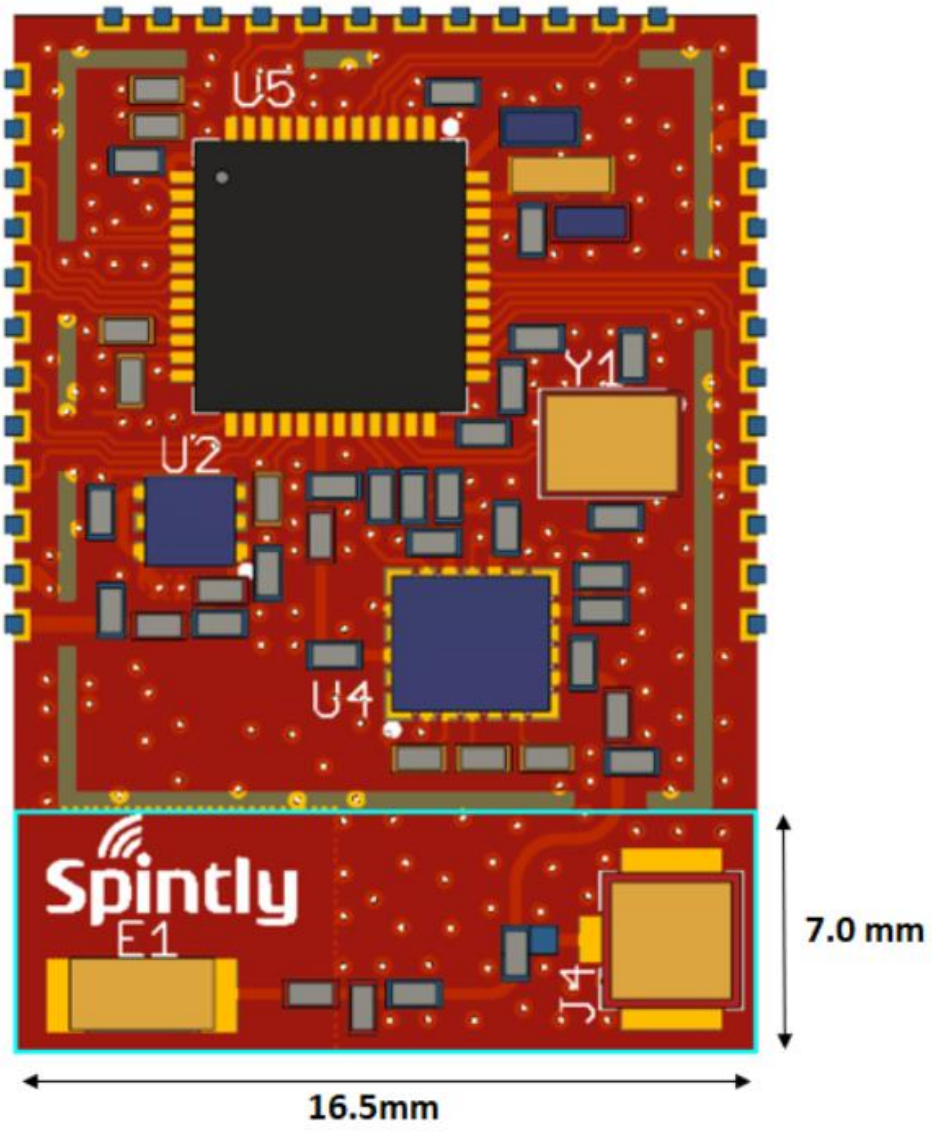
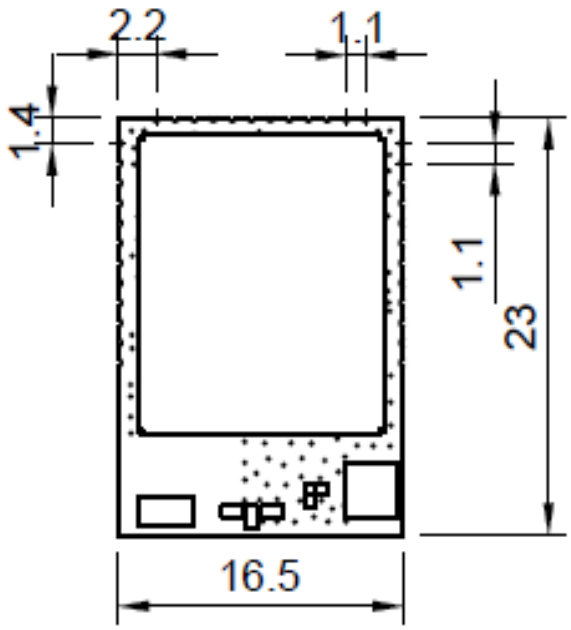


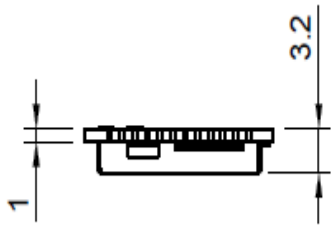
Figure 3: SPNYPM-52832-P02 PCB Antenna Size

13. Mechanical Specifications

13.1 36-SMD Package



TOP VIEW



SIDE VIEW

14. PCB Footprint and Dimensions

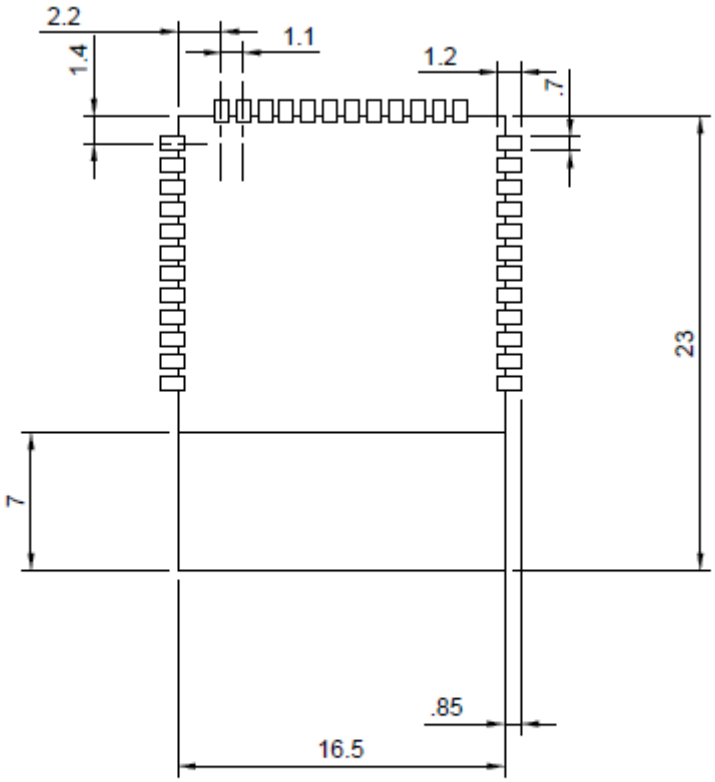


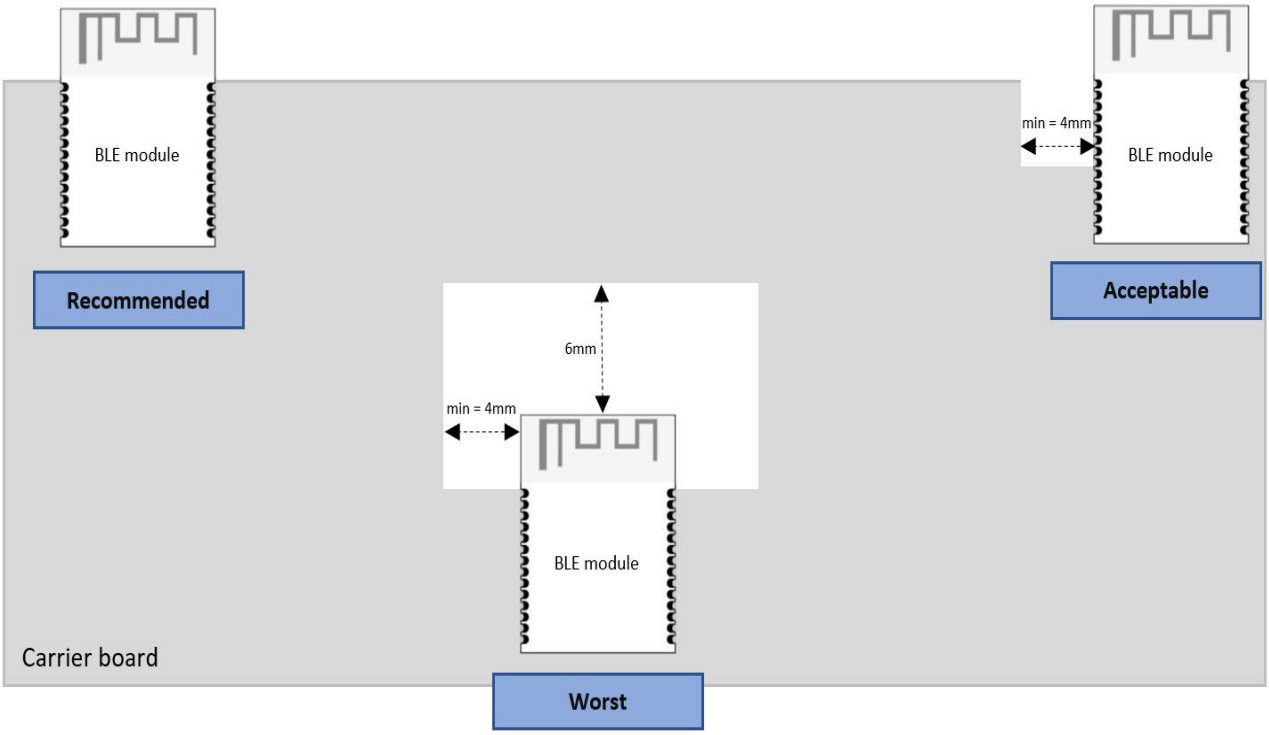
Figure 4: SPNYPM-52832-P02 PCB Footprint and Dimensions

14.1. Layout notes

To make sure wireless performance is at its best condition, please place the SPNYEM01 and SPNYEM02 module on the carrier board as below instructions and picture.

1. Placement of the antenna
The antenna area of module shall lay clearance completely and should not be blocked by the metal. Otherwise it will affect the antenna performance (As the picture indicated below).

2. Clearance
The area around the antenna shall have 4mm or more than 4mm clearance to reduce the influences for antenna.



15. Contact Information

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